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09/694,574	10/24/2000	Young Jin Oh	8733.007.01	2428

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MCKENNA LONG & ALDRIDGE LLP  
1900 K STREET, NW  
WASHINGTON, DC 20006

EXAMINER

QI, ZHI QIANG

ART UNIT PAPER NUMBER

2871

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Applicant(s)

09/694,574

OH ET AL.

Examiner

Mike Qi

Art Unit

2871

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 42,44-56 and 58-69 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 42,44-56 and 58-69 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/079,895.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 1.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Double Patenting*

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 42,44-56,58-69 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-41 of U.S. Patent No. 6,281,957 in view of US 5,852,485 (Shimada et al) and US 5,929,958 (Ohta et al).

Claims 42,44-56,58-69, especially claims 42 and 56, of this application have corresponding limitations with the claims 1-41, especially the claims 14 and 41 of the patent US 6,281,957 except a few wording are different, such as the limitations "a transparent first metal layer and a transparent second metal layer directly on the gate insulator", "a plurality of thin film transistors at crossing points of the gate and data bus lines", "a passivation layer formed substantially on the common line and thin film transistors" of this application; and the limitations "a transparent first metal layer including a plurality of first electrodes and a transparent second metal layer including a

plurality of second electrodes on the gate insulator”, “ a plurality of thin film transistors formed at respective crossing areas of the gate and data bus lines”, “ a passivation layer on the common line and the thin film transistors” of the patent US 6,281,957 are different, and that would be substantially obviousness-type double limitations.

Concerning the limitation “ a gate insulator on the first substrate” and “forming a gate insulator on the first substrate” that was a conventional structure of a liquid crystal display. Shimada discloses (col.1, line 25 – col.2, line 38; Figs.24-25) that on the lower glass plate (21) is formed the gate insulation film (23), and that is a conventional configuration of a liquid crystal display.

Concerning the dependent claims 44–55 and 58-69, all the limitations are related to an obviousness configuration of a liquid crystal display.

Claims 44 and 58, Shimada disclose (col. 11, line 15 – col.12, line21, Figs.1-3) that the TFT (122) includes a gate electrode (15) on the first substrate lower plate (120), a semiconductor layer (114) on the gate electrode (15), source electrodes (111) and drain electrodes (112) on the semiconductor layer (114).

Claims 45-46 and 59-60, Shimada disclose (col.11, lines 31-53; Figs.1-3) that the drain electrode (112) is connected to the picture element electrode (12 as the transparent first metal layer) through a connecting electrode (16) and a contact hole (17), the source electrode (111) is connected to the source line (14 as data line), and each counter electrode (as the second transparent metal layer) is connected to the common line through contact hole (col. 4, lines 23-26), i.e., the transparent second metal layer is connected to the common line.

Claims 47-48 and 61-62, Shimada disclose (col. 11, lines 32-53; Figs.1-3) that the connecting electrode (16) is connected to the picture element electrode (12), so that the electrode (16) also functions as pixel electrode, and the part of the electrode (16) overlapping the common line to form a storage capacitor. The part of the electrode (16) also overlapping the counter electrode (11) (Fig.3), so that forming another storage capacitor

Claims 49-50 and 63-64, Shimada disclose (col.12, lines 58-63; Figs.1-3) that the picture element electrode (12, 16) and the counter electrode (11) are formed of conductive material, e.g., ITO transparent conductive material, i.e., a transparent first metal layer (data electrode or pixel electrode) and a transparent second metal layer (counter electrode or common electrode).

Claims 51-52, 54-55 and 65-66,68-69, Shimada disclose (col.13, line 66 – col. 14, line 9; Figs 1-3) that a first alignment layer (116) on the first substrate (128) and the second alignment layer (117) on the second substrate (127), and the material for the alignment layer is polyimide.

Claims 53 and 67, Ohta discloses (col.19, lines 26-39, col.20, lines 26-37; Fig.7) that an in-plane liquid crystal display device comprising a black matrix (BM) layer on the second substrate (SUB2), a color filter (FIL) on the black matrix layer (BM) and a liquid crystal layer (LC) between the first and second substrates (SUB1, SUB2), such that to improve the contrast and to prevent external light goes to the semiconductor layer (AS) of the TFT, so that protecting the TFT, and using color filter to display color signal.

Therefore, it would have been obvious to those skilled in the art at time the invention was made to arrange the black matrix, color filters as claimed in claims 53 and 67 for improving the contrast and display color signal.

### ***Response to Arguments***

3. Applicant's arguments filed on Aug.26, 2002 have been fully considered but they are not persuasive.

Applicant's **only** arguments are as follows:

1) The references Shimada and Ota do not disclose the passivation layer formed substantially on the common line and thin film transistors as claimed in claims 42 and 56.

Examiner's responses to Applicant's **only** arguments are as follows:

1) The independent claims 42 and 56 of this application have corresponding limitations with the claims 1-41, especially the claims 14 and 41 of the patent US 6,281,957 except a few wording are different, such as the limitation "a passivation layer formed substantially on the common line and thin film transistors" of this application; and the limitation "a passivation layer on the common line and the thin film transistors" of the patent US 6,281,957 are different, and that would be substantially obviousness-type double limitations.

***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi  
August 31, 2003

  
ROBERT H. KIM  
SUPERVISOR OF PATENT EXAMINER  
TECHNOLOGY CENTER 2800